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HIGH PERFORMANCE WIDEBAND MSAG GAIN BLOCK/DRIVER AMPLIFIER MMICS USING MLP TECHNOLOGY

The multi-level plating (MLP) process has been used to develop a family of wideband, low noise, generic gain block and driver amplifier MMICs operating up to 20 GHz. MLP implementation provides significant performance improvements over standard MMIC processing techniques, especially with regards to bandwidth and gain. This article discusses salient features of the MLP process, including test data for multilayer microstrip lines, spiral inductors, 3 dB couplers and MLP-based MMIC amplifiers. The design approach and test data for several broadband MMICs, including a low noise amplifier, a single-bias gain block, and 0.25 W and 0.7 W driver amplifiers, are also described.

Wideband, low noise, generic gain block and driver amplifier MMICs have been developed using many different device technologies including MESFET, HBT and PHEMT. Among these, PHEMT-based MMIC technologies have achieved superior performance due to inherent device high frequency operation capability. In order to achieve superior performance similar to PHEMT technologies, multifunction self-aligned gate (MSAG®)-based MMICs are implemented using a multi-level plating (MLP) process. MLP utilizes multiple low dielectric constant polyimide and thick metallization layers atop the base GaAs. Designing with MLP allows for lower loss transmission lines or matching networks,[1–3] higher frequency operation and increased flexibility in the development of higher power components.

At the M/A-COM facility in Roanoke, VA, the MSAG MESFET process[4–9] is being used to develop low cost, high volume, high performance and highly reliable multifunction monolithic ICs for commercial and military applications. Because of its versatility in integrating low noise, power and high speed large-scale integration (LSI) functions on a single chip, the process has been named the

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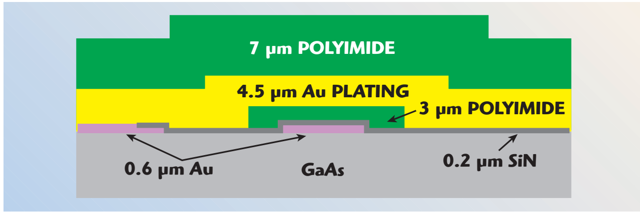
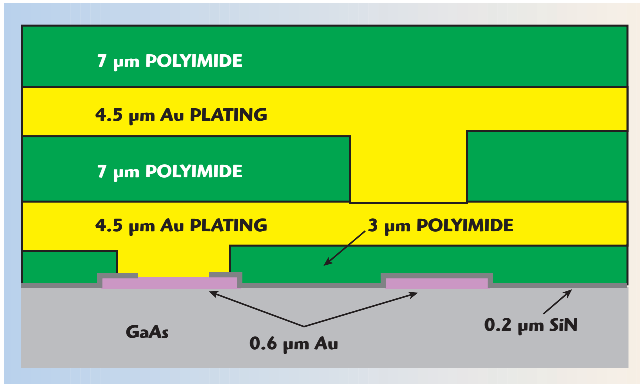
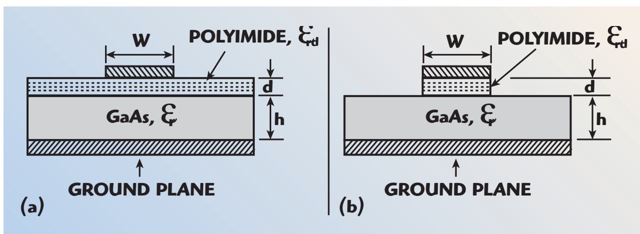


▲ *Fig. 1 Standard "Process 5" wafer cross-section.*



▲ *Fig. 2 Multi-level plating (MLP) process wafer cross-section.*



▲ *Fig. 3 Two modified microstrip line configurations.*

multifunction self-aligned gate process. The MSAG process eliminates the need for a gate recess, the single most important yield and reproducibility-limiting step. As each device type, which may include EFET, DFET, Schottky diode/limiter, low noise FET, switching FET, power FET and n' implants, is optimized for its respective function, it requires an additional mask. The MSAG process is available as a standard foundry service to outside users.

MULTI-LEVEL PLATING PROCESS

Figures 1 and ***2*** show stylized cross-section views of standard and MLP-processed GaAs wafers. A common design rule, set for core structures and common GaAs processing techniques, except for the MLP-unique elements, allows for simplified design, layout and processing.

There are two key differences between the standard and MLP-processed MMICs. The first is the addition of a second, 7 µm thick, low dielectric constant polyimide layer; the second difference is the addition of a second thick, 4.5 µm, gold metallization layer. These two additions provide the MLP advantages.

With the additional polyimide layer, a designer has the flexibility to locate transmission lines, known as multilayer microstrip lines, on polyimide up to 10 µm thick. The impedance of such lines can be increased by 40 to 60 percent — as compared to standard lines on the given base substrate. The high impedance capability of MLP is well

TABLE I

MEASURED CHARACTERISTICS OF MULTILAYER MICROSTRIP LINES WHEN GaAs SUBSTRATE THICKNESS IS 75 µm

Polyimide Thickness (µm)	Microstrip Width (µm)	Z_0 (Ω)	ε_{re}	α (dB/cm) @ 20 GHz
0	20	69.0	7.58	1.07
	50	50.0	8.26	0.83
	100	35.8	8.58	0.70
	150	28.1	9.15	0.61
3	20	81.0	5.32	0.85
	50	57.0	6.22	0.68
	100	41.0	7.10	0.55
	150	32.0	7.47	0.48
7	20	92.0	4.38	0.69
	50	64.1	5.08	0.50
	100	45.0	5.93	0.41
	150	35.5	6.45	0.37
14	20	105.0	3.70	0.55
	50	75.0	4.26	0.40
	100	53.0	4.90	0.35
	150	42.0	5.43	0.30

suited for implementing low loss matching networks and improving the bandwidth of passive components.

The additional thick metallization layer offers benefits as well, mostly in the area of DC current routing/high power design and extending the usage of passive components to lower frequencies. Most straightforwardly, the designer now has the flexibility to use 9 µm thick transmission lines. Current handling for such lines is 20 mA/µm.

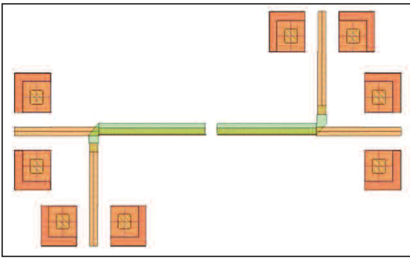
A second benefit of the additional thick metal layer is the option to create high current structures, such as spiral inductors. Previously, spiral inductors have been current limited, based on the width of the thin metallization underpass to access the center of the spiral, typically 2 mA/µm… as compared to 10 mA/µm for 4.5 µm thick lines. With MLP, a spiral inductor can be fabricated with 4.5 µm thick spirals and 4.5 µm thick underpasses.

The configuration of the multilayer microstrip line is shown in ***Figure 3***, where ε_r and ε_{rd} are the relative dielectric constants of the GaAs substrate and polyimide buffer layer, respectively, and h and d are their respective thicknesses. The thickness of the polyimide could be between 5 and 25 µm. However, the MLP process only allows polyimide thicknesses of 3, 7 and 10 µm. The microstrip conductor W has an approximate thickness of 4.5 µm. Typical dielectric constant values for GaAs and polyimide are 12.9 and 3.2, respectively. Measured results for the multilayer microstrip structure are summarized in ***Table 1***. As an example of the reduced loss characteristics of MLP, on a bare 75 µm GaAs substrate, a 50 Ω line is about 50 µm wide, whereas with a 10 µm polyimide layer atop the base GaAs, it is approximately 90 µm wide. The losses are 0.83 and 0.41 dB/cm, respectively, a 50 percent reduction for the 50 Ω line on polyimide. Further improvement may be obtained by etching away the surrounding polyimide, so that more of the microstrip is surrounded by air. This configuration is also compatible with multi-level plating MMIC fabrication processes.

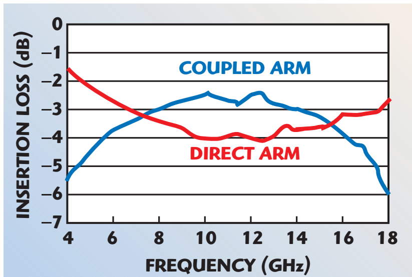
TABLE II

COMPARISON OF SEVERAL 6.7 nH INDUCTORS FOR BEST FIGURE OF MERIT INDEX

Parameter	Standard Inductor	Multi-layer Inductor	3D Inductor
f_{res} (GHz)	5.0	6.4	4.43
Q	22.0	33.0	28.5
Area (mm^2)	0.193	0.193	0.084
FMI (GHz/mm^2)	5.7	10.9	15.03



▲ *Fig. 4 Physical layout of the 3 dB asymmetric broad side coupler.*



▲ *Fig. 5 Measured performance of the 3 dB coupler.*

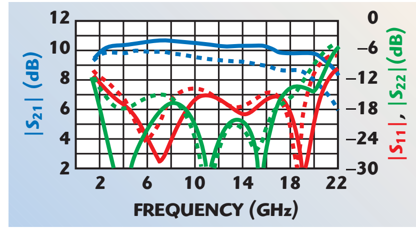
A family of 6.7 nH inductors was also characterized, and their figure of merit indexes (FMI) is compared in ***Table 2***. FMI is defined as

$$\text{FMI} = \frac{Qf_{res}}{\text{Inductor Area}} \tag{1}$$

where

f_{res} = self-resonance frequency

The inductors selected are a standard inductor with thin metal underpass, a MLP multilayer inductor with 9 µm thick spiral metallization and a 3-D inductor. The Q values are obtained at the maximum Q frequency. It is easily noted that the 3-D structure has the best FMI. This is because of its reduced area. A trade-off of this inductor type is that it has the lowest resonance frequency due to higher inter-level capacitances. The Q factor



▲ *Fig. 6 Predicted performance of a 2 to 20 GHz distributed amplifier using a standard "Process 5" (dashed lines) and MLP (solid lines) processing.*

for the 3-D inductor is about 23 percent higher than for the standard inductor but about 16 percent lower than for the multilayer inductor using thick metallization. The FMI for the 3-D inductor is about 2.6 times larger than for the standard inductor.

A final example of the benefits of MLP is a broadband 3 dB coupler, which is required in many microwave applications. MLP is also suitable to realize tight directional couplers on GaAs substrates. A 3 dB asymmetric broadside coupler was developed using the MLP process on a 75 µm thick GaAs substrate. ***Figure 4*** shows the top-sectional view of the broadband coupler, which operates over the 7 to 15 GHz frequency range. The physical length of the coupler is 3000 µm. The bottom and top conductor line widths are 40 and 60 µm, respectively, resulting in a lower dissipated loss than for a Lange coupler on GaAs. As shown in ***Figure 5***, the measured insertion loss in the coupled and direct ports are 3.3 ± 0.5 dB and 3.5 ± 0.5 dB, respectively. The measured return loss was better than 18 dB.

The MLP process results in improved performance in MMIC passive components including couplers, filters, dividers/combiners and transformers, and also allows the realization of new MMIC components including thin film microstrip, multi-level inductors, tight couplers and baluns.

DISTRIBUTED AMPLIFIERS USING THE MLP PROCESS

At the circuit level, improvements in performance can be achieved using very high impedance lines (microstrip lines on 10 µm polyimide) in the gate and drain equivalent transmission lines of a distributed amplifier, using low loss matching networks at the output of a power amplifier, using high current carrying capacity inductors in matching networks and using 9 µm thick conductors instead of 4.5 µm thick conductors having twice the width. An approximate expression for the small-signal gain of a distributed amplifier is given by[10]

$$G \cong \frac{g_m^2 n^2 Z_0}{4}\left[1 - \alpha_g \ell_g \frac{n}{2}\right]^2 \tag{2}$$

where

n = number of FETs
g_m = transconductance per FET
Z_0 = characteristic impedance of the gate line
α_g = attenuation constant of the gate line
ℓ_g = length of gate line per unit cell

In this expression, a constant characteristic impedance and a constant unit line length have been assumed. Also, the drain line losses are neglected. Equation 2 shows that, for higher gain, one needs higher Z_0 and lower α_g. As previously shown, MLP provides both these features.

As an example of the performance benefit MLP provides for wideband MMICs, ***Figure 6*** shows the predicted performance of a pair of 2 to 20 GHz distributed amplifiers, one designed using standard Process 5 techniques and the other implemented in MLP. As is easily noted, approximately 1.5 dB additional gain is provided by the MLP design at 20 GHz. Thus, MLP can be used to either increase gain for a given bandwidth, or provide additional bandwidth for a given amount of gain.

In the following, examples of distributed amplifiers developed using MSAG FET with the MLP process are described. In these MMICs, the gate and drain microstrip conductors are on a 10 µm thick polyimide layer atop the GaAs substrate. The circuits were designed using small-signal models for the FET devices and matched to 50 Ω at the input and output.

2 to 20 GHz Distributed LNA (Self-biased)

Figure 7 shows the physical layout of a 2 to 20 GHz distributed LNA, incorporating six 150 µm 5N (low noise) FETs. The circuit was designed for low noise figure and high gain using a low noise FET model. A single supply operation is provided through the use of on-chip self-biasing networks. The value of the resistor between the source of the device and ground is selected to bias the device at 0.25 I_{DSS} to provide

a trade-off between minimum noise figure and high P1dB. The drain supply voltage is 5 V. The chip size is 3 × 1.6 mm.

Figures 8 and ***9*** show the measured LNA gain and noise figure, and P1dB, respectively. The current under drive increases from 75 mA at the Q-point to about 110 mA at the P1dB compression point. The measured return loss was better than 10 dB over the 2 to 20 GHz frequency range.

2 to 18 GHz Distributed Amplifier Driver (Self-biased)

Figure 10 shows the physical layout of a distributed driver amplifier (DA), designed for the 2 to 18 GHz frequency band. It is comprised of five 5N FETs, each having a 300 µm gate periphery. The circuit was designed for high P1dB and high gain while providing a good match to 50 Ω at the input and output. A single supply operation is provided through the use of on-chip self-biasing networks. The nominal drain supply voltage is 5 V; however, on-chip voltage drop resistors allow variable supply voltage from 5 to 8 V. The chip size is 3 × 1.7 mm. ***Figure 11*** shows the measured gain and return loss; ***Figure 12*** demonstrates the saturated power at different drain biases.

2 to 18 GHz Distributed Power Amplifier

This is another DA, designed for higher power level. It uses the same approach as discussed previously. This topology employs five 300 µm 5A (power) FETs biased at 8 V. The physical layout of this circuit is shown in ***Figure 13***. The MMIC is over-sized at 3.0 × 1.7 mm due to the limitations of being in a development mask. In a production mask, the final chip size would be 2.3 × 1.4 mm. ***Figures 14*** and ***15*** show the measured gain and noise figure, and output P1dB, respectively.

2 TO 8 GHz DRIVER AMPLIFIER

Another useful feature of MLP is to create high current inductors for broadband and compact designs.[11] In

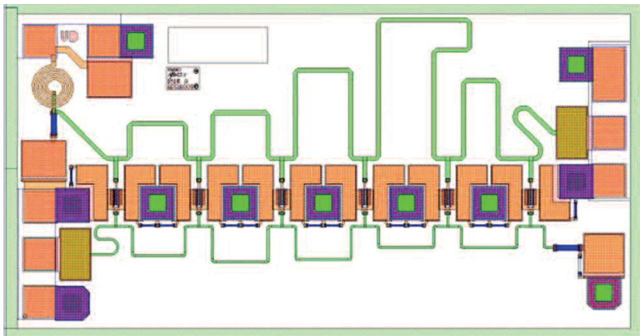


Fig. 7 Layout of a 2 to 20 GHz self-biased distributed LNA.

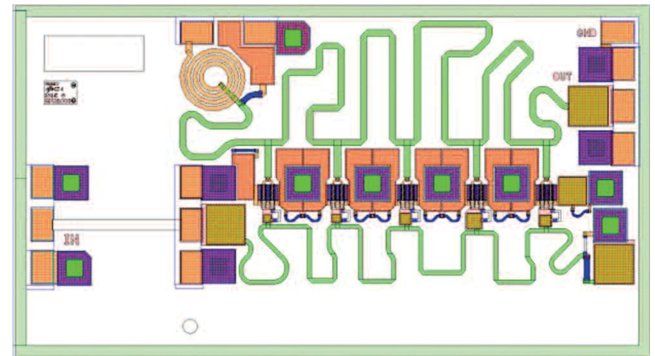


Fig. 13 Layout of a 2 to 18 GHz distributed power amplifier.

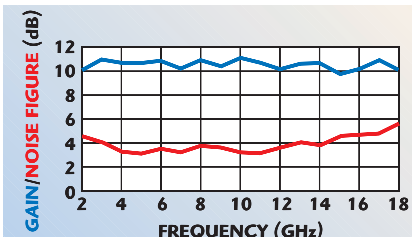


Fig. 8 Measured gain and noise figure of self-biased 2 to 20 GHz distributed LNA.

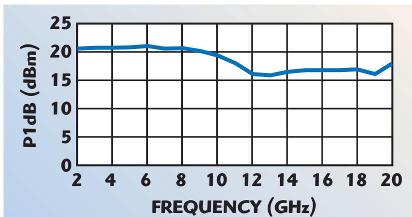


Fig. 9 Measured P1dB of self-biased 2 to 20 GHz distributed LNA.

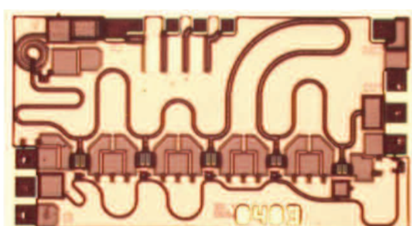


Fig. 10 A 2 to 18 GHz self-biased distributed driver amplifier.

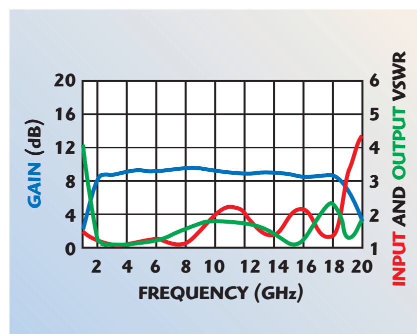


Fig. 11 Small-signal gain, and input and output VSWR at $V_D = 5$ V of the distributed amplifier driver.

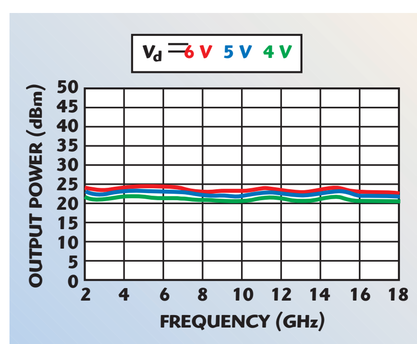


Fig. 12 Saturated output power of the distributed amplifier driver as a function of frequency and drain voltage.

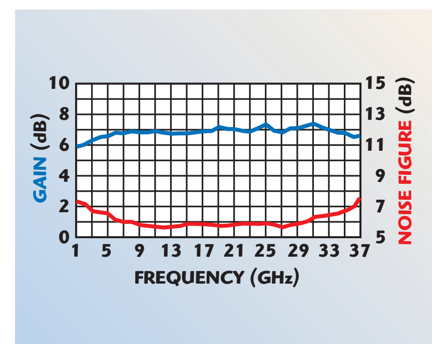


Fig. 14 Measured gain and noise figure of the 2 to 18 GHz distributed power amplifier.

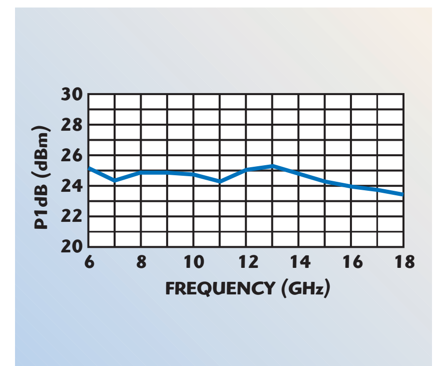
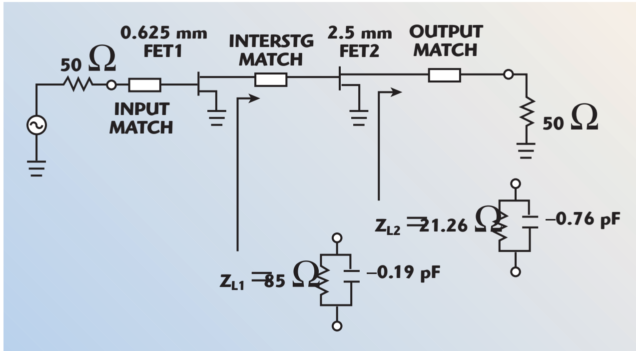


Fig. 15 Measured P1dB of the 2 to 18 GHz distributed power amplifier.



▲ *Fig. 16 Schematic of a two-stage driver amplifier.*

this section, a broadband 0.7 W driver amplifier developed using MLP inductors is discussed.

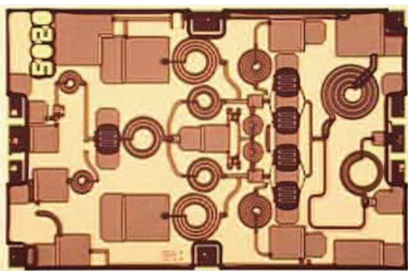
Traditionally, a driver amplifier is designed based on the loadline method.[12–15] The design of the two-stage broadband MMIC driver amplifier was based on a design methodology using small-signal, nonlinear FET models and loadpull data obtained at the operating bias point. The operating point of the amplifier was selected for class-AB operation (0.30 I_{DSS}) of the device in order to obtain the best compromise of power output, gain, PAE, linearity and variable power supply operation over the 2 to 8 GHz frequency range.

In this design, the loadline technique is used initially to optimize the circuit parameters. The optimum load impedances Z_{L1} and Z_{L2} at the drain of the first and second stage FETs, necessary to realize the maximum output power and PAE, are shown in ***Figure 16***. Then, the design is simulated using the nonlinear model to calculate the power compression of each stage and the output power and PAE as a function of input power. Since it is very difficult to optimize the matching networks to the required load impedances over wide bandwidths, using nonlinear models, the above design process is repeated so that an optimum solution for simultaneous match to the load impedances at the drain of each FET and best gain, power and PAE are achieved.

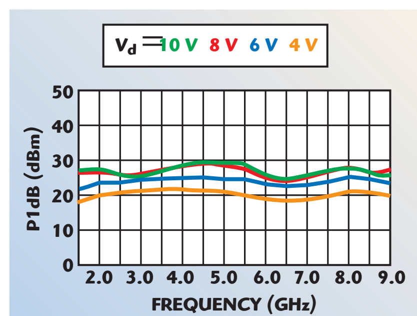
The input stage, which has a limited gain compensation network, was designed for good input match as well as for maximum power transfer at the high frequency end. The interstage matching network was designed to provide a flat gain response and deliver enough power to the output stage FETs for achieving overall maximum output power and PAE. The output matching elements were selected to provide an optimum load match with minimum insertion loss, since efficiency and output power are reduced to a great extent by a passive loss. Both stages, as well as the complete amplifier, were designed to be unconditionally stable over 3 to 10 V drain power supply voltage and 0.25 to 0.50 I_{dss} drain current. Experience has shown that for MSAG FETs, standard even-mode (K > 1) and odd-mode stability analyses are adequate to avoid microwave oscillations. However, under large-signal condition and pulsed operation, it is necessary to use worst-case K-factors greater than 1 when S-parameter data is used for various bias conditions from V_{ds} = 3V, 0.50 I_{dss} to V_{ds} = 10V, 0.25 I_{dss}. This approximately replicates the envelope a full cycle of the input signal experiences during the large signal and pulsed operation. It was found that imposing a K > 2.0 condition, for V_{ds} = 10V and 0.25 I_{dss} small-signal S-parameters, is about what is necessary to ensure K > 1 under all conditions.

Figure 17 shows the photograph of the two-stage 0.7 W power output driver amplifier. The chip size is 3 × 2 mm.

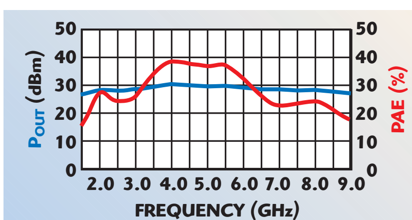
Typical CW measured P_{out} and PAE for MMIC chips on Cu-W carriers at V_{DS} = 8V and P_{in} = 18 dBm are shown in ***Figure 18***. The amplifier has greater than 28.5 dBm power output and better than 24 percent PAE over the 2 to 8 GHz frequency range. ***Figure 19*** depicts P1dB power levels at various drain voltages. The variations of small-signal gain and input VSWR as a function of frequency are shown in ***Figure 20***. The input VSWR is better than 2:1 over the 1.5 to 8.4 GHz range.



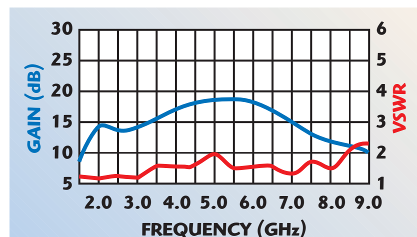
▲ *Fig. 17 A 2 to 8 GHz, 0.7 W driver amplifier.*



▲ *Fig. 19 P1dB of the 2 to 8 GHz driver amplifier as a function of drain voltage.*



▲ *Fig. 18 P_{out} and PAE of the 2 to 8 GHz driver amplifier at V_D = 8 V P_{IN} = 18 dBm.*



▲ *Fig. 20 Small-signal gain and input VSWR of the 2 to 8 GHz driver amplifier at V_D = 8 V.*

CONCLUSION

A family of wideband, low noise, generic gain block and driver amplifier MMICs for commercial and military applications has been developed. Using MLP processing, higher performance and higher frequency operation are achieved. ■

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